

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
14 April 2005 (14.04.2005)

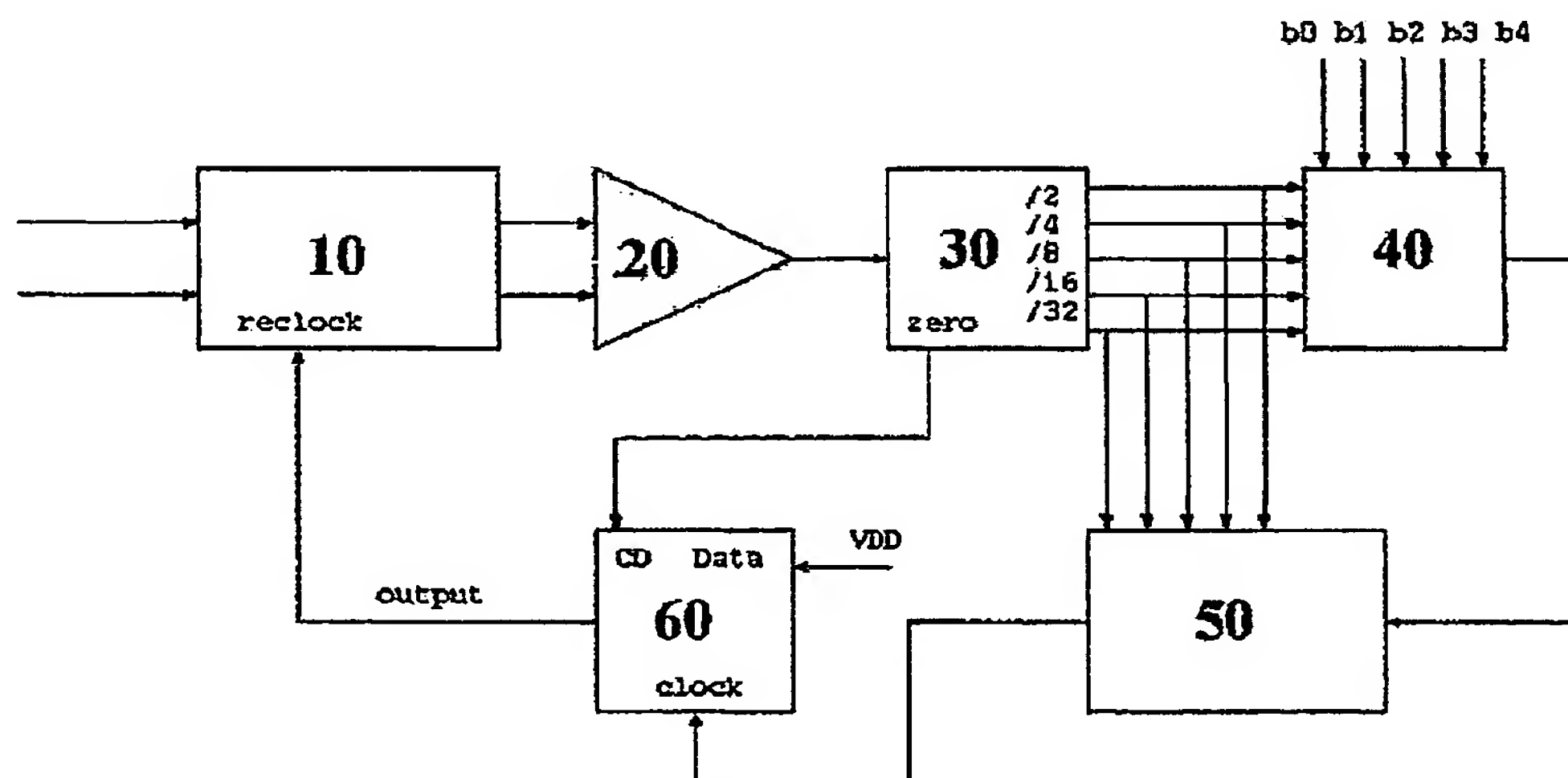
PCT

(10) International Publication Number
WO 2005/034358 A1

- (51) International Patent Classification⁷: **H03L 7/197, H03K 23/66**
- (21) International Application Number: **PCT/IB2004/051894**
- (22) International Filing Date: **28 September 2004 (28.09.2004)**
- (25) Filing Language: **English**
- (26) Publication Language: **English**
- (30) Priority Data: **03103631.2 1 October 2003 (01.10.2003) EP**
- (71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).**
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **LEENAERTS, Dominicus, M., W. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). PAVLOVIC, Nenad [YU/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). MIS-TRY, Ketan [GB/GB]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).**
- (74) Agent: **ELEVELD, Koop, J.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).**
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): **AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.**
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): **ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).**
- Published:
— with international search report

[Continued on next page]

(54) Title: **PHASE-SWITCHING DUAL MODULUS PRESCALER**



(57) Abstract: A phase-switching dual modulus prescaler having a dual modulus divider is provided. Said divider comprises a first and second divide-by-2 circuit (A;B), wherein said second divide-by-2 circuit (B) is coupled to the output of said first divide-by-2 circuit (A) and at least said second divide-by-two circuit (B) comprises a four phase output each separated by 90°. A phase selection unit (PSU) is provided for selecting one of the four phase outputs (I_p , I_n , Q_p , Q_n ; IN_i , IN_{ni} , IN_q , IN_{nq}) of the second divide-by-2 circuit (B). Moreover, a phase control unit is provided for providing control signal (C_1 , NC_0 ; C_2 , NC_2 ; C_3 , NC_3) to the phase selection unit, wherein the phase selection unit (PSU) performs the selection of the four phase outputs (I_p , I_n , Q_p , Q_n ; IN_i , IN_{ni} , IN_q , IN_{nq}) according to the control signals (C_0 , NC_0 ; C_1 , NC_1 ; C_2 , NC_2). Said phase selection unit (PSU) is implemented based on direct logic. The implementation of the phase selection unit based on direct logic enables a higher speed and saves area on the chip.

WO 2005/034358 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.